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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,284	02/13/2002	Hirokazu Yamagata	740756-2345	3476

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EXAMINER
FOONG, SUK SAN

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/073,284	YAMAGATA ET AL
	Examiner	Art Unit
	Suk-San Foong	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 25-82 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 25-82 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 2/23/02 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,8
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. The restriction between 1st species and 2nd species is withdrawn because the species are not now seen to be patentably distinct.

Drawings

2. Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 40 and 45 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no description in the specification as originally filed of plasma treating the surface of an interlayer insulating film. (See 1242 OG 168 p. 172).

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 27, 32, 37, 41, 42, 47, 66 and 71 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 27, line 2, and subsequent claims, it appears that "more kinds of" should be deleted.

7. Claim 27, lines 3-4, it is unclear what is recited through the term "rare gas." It appears that "rare gas" should be replaced by--noble gas--; unless another step is intended.

8. Claims 41 and 42, line 2, it appears that--the--should be inserted after "wherein."

9. Claims 66 and 71, line 8, it appears that line 8 should be deleted.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 25-28, 30-33, 35-38 and 40-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in combination with Yamada ('179), Inoue et al. ('206), So et al. ('905) and Garcia et al. ('369).

AAPA admits to a process substantially as claimed to have been known prior to applicant's invention (See Instant p. 2-4 and Fig. 2) and further recognizes the problem of transferring semiconductor wafer with partially finished circuits such as TFT from one clean room to another clean room for further processing a light emitting portion on the semiconductor wafer.

The admitted prior art process does not include forming an interlayer insulating film over the TFT structure.

Yamada teaches a method of forming organic EL (electroluminescent) display which includes forming a TFT structure including active layer 33 and gate electrodes 31 over semiconductor substrate 10 (Col. 5, lines 36-63, and Fig. 4A), subsequently forming interlayer insulating film 14 over the TFT structure (Col. 5, lines 63-67), subsequently forming first

organic resin insulating film 17 over substrate 10 (Col. 6, lines 2-4), then wiring line through first insulating film 17 (Col. 6, lines 24-29), and then performing subsequent steps for forming the light emitting portion of the display device (Fig. 4B).

It would have been within the scope to one ordinary skill in the art to combine both teachings because it would enable forming the TFT and light emitting portion of the display device of the admitted prior art process to be performed.

The combination process does not include performing heat treatment on the anode.

The combination process does not include performing heat treatment on the resin insulating film.

The combination process does not include performing plasma treatment on the bank.

Inoue et al. discloses a method of forming thin film transistors which includes forming a TFT structure such as gate electrode 2, common electrode 3, a-Si film 5 and etc. (Col. 6, lines 28-33, and Fig. 1A), then applying resin insulating film 10 over the TFT structure and baking resin insulating film 10 (Col. 6, lines 33-34 and 55-58), subsequently etching through resin insulating film 10 to form contact hole 11 (Col. 6, lines 58-61), then performing surface treatment on resin insulating film 10 through plasma treatment using gas such as nitrogen (Col. 3, lines 46-51, Col. 6, line 66 to Col. 7, line 3, Table 1 and Fig. 1B), subsequently forming pixel electrode or anode 13 to electrically connect to the thin film transistor structure, and then conducting heat treatment on anode 13 (Col. 7, lines 5-16).

It would have been within the scope to one ordinary skill in the art to combine the teachings of the admitted prior art process with Inoue et al. because it would enable formation of anode 205 of the admitted prior art process to be performed.

It would have been within the scope to one ordinary skill in the art to combine the teachings of the admitted prior art process with Inoue et al. because it would enable heating and plasma treating the resin insulating material for formation of bank 208 of the admitted prior art process to be performed and obtain further advantage of eliminating residues (Inoue et al. Col. 3, lines 51-54).

The combination process does not include forming a second insulating film over the anode.

So et al. teaches a method of forming organic electroluminescent devices which include forming anode 14 over substrate 12 (Col. 2, lines 52-58, and Fig. 1), subsequently depositing insulating film 16 over anode 14 (Col. 2, lines 64-65), then depositing organic compound layer 18 insulating film 16 (Col. 3, lines 12-17 and 21-25), and subsequently depositing cathode 22 on organic compound layer 18 (Col. 5, lines 33-34 and 66-67).

It would have been within the scope to one ordinary skill in the art to combine the combination process with So et al. because it would enable formation insulating film in the light emitting element of the admitted prior art process to be performed and obtain further advantage of improving device stability (So et al., Col. 5, lines 61-65).

The combination process does not include wiping the anode.

Garcia et al. discloses that it is a common practice where a semiconductor wafer is thoroughly clean, rinse and dry after completion of each layer, used in forming electrically active regions on the wafer's surface, to remove contaminants from the surface (Col. 1, lines 18-36). Garcia et al. further discloses scrubbing the surface of the semiconductor wafer using a PVA-based porous material (Col. 4, lines 16-21).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Garcia et al. with the combination process because it would enable wiping anode 205 of the admitted prior art process to be performed and obtain further advantage of removing contaminants (Garcia et al., Col. 1, lines 34-35).

13. Claims 29, 34, 39 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in combination with Yamada ('179), Inoue et al. ('206), So et al. ('905) and Garcia et al. ('369) as applied to claims 25-28, 30-33, 35-38 and 40-43 above, and further in view of Farber et al. ('684).

The combination process does not disclose the wiping step is for leveling the surface of the anode.

Farber et al. discloses a method of cleaning semiconductor wafer by scrubbing the wafer using PVA-based porous materials (Col. 5, lines 2-6) thereby removing contaminants, etching the surface of the wafer or buffing the surface (Col. 5, lines 28-32).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Farber et al. with the combination process because it would enable the step of cleaning the semiconductor wafer of the combination process to be performed.

14. Claims 45-53, 56-58, 61, 62, 64, 65, 67, 74-80 and 82 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Yamada ('179), Inoue et al. ('206), So et al. ('905) and Garcia et al. ('369) further in view of Farber et al. ('684) as applied to claims 25-

28, 30-33, 35-38 and 40-43 and 29, 34, 39 and 40 above, and further in view of Satoh et al. ('334) the combination alone or in view of Sakata et al. ('584).

The combination process does not include forming the film for protecting underlying thin film transistor from contamination and electrostatic discharge damage.

AAPA recognizes the problem of transferring semiconductor wafer from one clean room to another clean room as described above.

Alternatively, in the event that applicant is not admitting the observations stated in paragraph bridging instant pages 3 and 4 to have been known prior to applicant's invention, Sakata et al. discloses that in a typical process for manufacturing liquid crystal device at least 80 manufacturing steps are required wherein, between these manufacturing steps, half-finished TFT-LCD substrates are exposed to the atmosphere for several hours before being transferred to a clean room for further processing (Col. 1, lines 30-45). Consequently, contaminants are deposited on surface of the LCD substrate and, thereby, compromising the efficiency of the device (Col. 1, lines 47-67).

Satoh et al. discloses a method of forming protective film on semiconductor wafers which includes applying a protective film of organic insulating material over device side of a semiconductor substrate for protection against deposition of dusts or the like present in the atmosphere (Col. 2, lines 3-10, Col. 3, lines 57-64), and subsequently removing the protective film from the surface of the semiconductor substrate (Col. 4, lines 22-26).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Satoh et al. with the combination process because it would enable transferring the semiconductor wafer from one clean room to another clean room of the admitted prior art

process and obtain further advantage of preventing contamination such as dusts (Satoh et al., Col. 2, lines 6-8).

Examiner takes official notice that baking resin insulating material was known at the time of applicant's invention to remove solvents and expel gases.

It would have been within the scope to one ordinary skill in the art to combine the teachings of the known process with the combination process because it would enable formation of bank 208 of the admitted prior art process to be performed.

Examiner takes official notice that organic insulating material as recited in claim 56, for example, were known to be used in semiconductor processing including depositing and removal of layers.

In view of the suggestion in Satoh et al. of using organic insulating film and in view of suitable materials as described in Col. 1, lines 41-48 of Satoh et al., it would have been within the scope to one ordinary skill in the art to combine the teachings of known teachings with the combination process to enable formation of the protective film in the combination process to be performed.

15. Claims 54, 55, 59, 60, 63, 66, 68, 69-73, 79 and 81 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Yamada ('179), Inoue et al. ('206), So et al. ('905) and Garcia et al. ('369) further in view of Farber et al. ('684) and further in view of Satoh et al. ('334) as applied to claims 25-28, 30-33, 35-38 and 40-43, and 29, 34, 39 and 40, and 45-53, 56-58, 61, 62, 64, 65, 67, 74-80 and 82 above, and further in view of Montgomery et al. ('995).

The combination process does not disclose that the protective film is comprised of organic conductive material selected from the group as recited in claim 54, for example.

Montgomery et al. discloses a method of forming protection film 20 such as organic conductive layer comprised of material such as polyaniline by spin coating over semiconductor substrate 12 for preventing contaminants when resist 16 formed on substrate 12 is exposed during storage, for example, (Paragraph [0009]) wherein protection film 20 is removable in subsequent processing steps (Paragraph [0025], and Fig. 1).

Examiner takes official notice that etchants and conditions were known to remove the films selectively as recited.

In view of the suggestion in Satoh et al. of using suitable materials as described at Col. 1, lines 41-48, it would have been within the scope to one ordinary skill in the art to combine the teachings of Montgomery et al. and the known teachings with the combination process because it would enable formation and removal of the protective film of the combination process to be performed.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

SF
January 30, 2003

George Fourson
Primary Examiner
Art Unit 2823